

PATENT ABSTRACTS OF JAPAN

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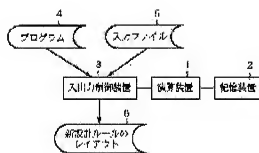
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(54) COMPACTOR FOR SEMICONDUCTOR INTEGRATED CIRCUIT LAYOUT, COMPACTION METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT LAYOUT, AND RECORDING MEDIUM

(57)Abstract:

PROBLEM TO BE SOLVED: To solve such a problem that circuit performance before the execution of compaction is damaged especially in the layout of an analog circuit by changing timing of signal delay since a circuit pattern 70 of semiconductor integrated circuit(IC) layout is one-sidedly located unintentionally in the layout when the compaction is executed.

SOLUTION: This device is provided with a location area dimension estimating means for calculating the dimension of the location area of constitutive parts after the execution of compaction, a coordinate calculating means for equal location for calculating coordinates for equal location for partitioning the location area at equal intervals after the execution of compaction on the basis of the dimension of this location area, and an equal location means for locating the respective constitutive parts inside the equal location area on the coordinates for equal location after the execution of compaction when executing the compaction to the semiconductor IC



layout.

LEGAL STATUS

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